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Techniques for Power and Reliability Optimization of CMOS Logic

By Diril, Abdulkadir Utku

Condition: New. Publisher/Verlag: LAP Lambert Academic Publishing | Power optimization, soft error tolerance improvement | As the transistors became smaller in size and the systems became faster, issues like power consumption, signal integrity, soft error tolerance, and testing became serious challenges. There is an increasing demand to put CAD tools in the design flow to address these issues at every step of the design process. First part of this research investigates circuit level techniques to reduce power consumption in digital systems. In second part, improving soft error tolerance of digital systems is considered as a trade off problem between power and reliability and a power aware dynamic soft error tolerance control strategy is developed. The objective of this research is to provide CAD tools and circuit design techniques to optimize power consumption and to increase soft error tolerance of digital circuits. Multiple supply and threshold voltages are used to reduce power consumption. Variable supply and threshold voltages are used together with variable capacitances to develop a dynamic soft error tolerance control scheme. | Format: Paperback | Language/Sprache: english | 108 pp.



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